The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MOSHE GEFEN,
SHUKA ZERNOVIZKY and AMIR BAN

Appeal No. 2005-1551
Application 09/629,966

ON BRIEF

Before THOMAS, HAIRSTON, and DIXON, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board, the claims on appeal having been twice rejected, within 35 U.S.C. § 134 from the examiner's rejections of claims 1, 3 through 6, 10, 13, 14 and 16 through 30.

Representative claim 1 is reproduced below:

1. A system that executes code while processing data operations using a non-volatile memory device, comprising:

host for accessing said memory device;

non volatile array for holding code and data of said system;

non volatile device circuitry for controlling content and activity of said non volatile array; and

logic circuit, separate from said host, for enabling automatic suspending and/or automatic resuming of operations in response to a read request from said host.

The following references are relied on by the examiner:

Miller	4,491,790[1]	Jan. 1, 1985
See et al. (See)	6,189,070	Feb. 13, 2001 (filed Aug. 28, 1997)

Claims 29 and 30 stand rejected under the written description portion of 35 U.S.C. § 112, first paragraph. Claims 1, 3, 4, 6, 10, 13, 14 and 16 through 30 stand rejected under 35 U.S.C. § 102(e) as being anticipated by See. Claim 5 stands rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon See in view of Keeley.

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[1] The U.S. Patent No. of 4,491,790 bears a patentee's name of Miller rather than Keeley as asserted by the examiner. The most recent papers in the record do not bear any effort by the appellants and the examiner to correct this rather apparent recitation of an incorrect patent number.

Rather than repeat the positions of the appellant and the examiner, reference is made to the Brief (no Reply Brief has been filed) for appellants' positions, and to the Answer for the examiner's positions.

OPINION

We affirm-in-part since we sustain the examiner's rejection of the claims under 35 U.S.C. § 112, but reverse the rejections of the claims under 35 U.S.C. § 102 and 35 U.S.C. § 103.

Turning first to the rejection of claims 29 and 30 under the written description portion of 35 U.S.C. § 112, first paragraph, we sustain this rejection. These claims were not original claims but were filed in the after final response by appellants in the Amendment filed as Paper No. 7, on February 23, 2004. These claims were presented at page 7 of this Amendment with corresponding remarks at pages 13 and 14.

The examiner's view is essentially that there is no clear support in the original disclosure for suspending/resuming operations being "effected only by the memory device." On the one hand, the examiner recognizes that there is support for the

memory device controlling the suspend/resume processes, but that there is no explicit support for only the memory device effecting the processing. Answer, page 3.

For their part, appellants argue at pages 9 and 10 of the Brief that the Specification does describe how the suspending and resumption of a program/erase operation is managed exclusively by automatic suspend logic 16 and automatic resume logic 27 illustrated in Figure 4 as components of the memory device illustrated there, and as discussed in the specification as filed beginning at page 8, line 14, through the end of the specification. For the moment, we observe that the claims do not recite that the program and erase operations are managed exclusively by the respective suspend and resume logics in Figure 4. Thus, the actual claim language is not coextensive with the arguments at page 9 of the Brief.

In response, the examiner correctly observed at page 10 of the Answer:

> [I]s it not the CPU making a request over CPU bus 20 and bus logic 21 that initiates the suspend and resume logic? This would seem to be supported by the claimed parts (b) and (c) in claim 24, reading "during said operation, requesting a read operation, ***by the host;*** and ***in response to said request***, suspending said

> operation, by the memory device." Much like the Applicants' own arguments beginning at the bottom of page 14 of the Brief, even though the only hardware recited explicitly in the specification for suspending and resuming is inside the memory device of figure 4, it is clear that the CPU (or host) participates actively in the automatic suspending and resuming operations. Therefore, for the reasons given above, there does not appear to be explicit support for the claimed limitations of suspending/resuming being effected ***only*** by the memory device.

The recitation of "effected only by the memory device" excludes functional/state operations external to the memory device unit as not causing or effecting the function of suspending and resuming. As the examiner well explains, this is not the case according to the disclosure. The examiner is correct in assessing that the predicate is the read operation from the CPU in the context of all the claims on appeal which is consistent with the overall disclosure. The CPU read request "effects" or otherwise causes the suspension operation and the absence of the CPU read request causes or "effects" the resumption of the erasing/programming (writing) operations. To be consistent with the specification as disclosed, the recitation should have recited that the respective suspending and resumption operations are automatically executed by or on the memory device

after the CPU issues the read request in accordance with the teachings at specification page 6, lines 7 through 9; page 8, line 14; page 9, lines 1 and 2 and line 15; and, finally, the Abstract's first sentence at page 15. Therefore, there is ample basis to sustain the examiner's rejection of claims 29 and 30 under the written description portion of 35 U.S.C. § 112, first paragraph.

On the other hand, we reverse the rejection of each independent claim 1, 13, 14, 16, 17 and 24 under 35 U.S.C. § 102 and, consequently, the separate rejection of dependent claim 5 under 35 U.S.C. § 103.

We observe initially that each independent claim on appeal recites either the suspension and resuming operations or only the suspending operations being in some manner "in response to a read request from said host." We therefore are in essential agreement with appellants' position set forth at page 15 of the Brief on Appeal which we reproduce here:

> Furthermore, the Examiner did not even address the second aspect of the present invention, as recited in independent claims 1, 13, 14, 16, 17 and 24, that distinguishes the present invention from the teachings of See et al. '070. Flash device 410 of See et al. '070 suspends an erase

> operation in response to an erase suspend command not in response to a read command. Flash device 410 of See et al. '070 suspends a programming operation in response to a program suspend command, not in response to a read command. By contrast, the memory device of the present invention suspends erase and programming operations in response to read commands/requests.

Although the Examiner's selection, arguments and noted portions of See would appear to be compelling evidence of anticipation of the subject matter of the independent claims on appeal, this reference does not anticipate the subject matter of each of these claims. From our detailed consideration of See, it is an interrupt function to the CPU of See that directly causes the suspension of a non-read operation, such as an erase/program (write) operation, which in turn leads to a read operation of the flash memory in this reference. The claims on appeal, on the other hand, require that the read request/command itself causes the suspend operation. As illustrated in Figure 4B of See, once an interrupt has occurred according to element 540, a suspend operation occurs in element 542, where a read mode is then executed in element 550. It is this read operation that is a vectored interrupt or a read function directly to the flash memory to service the interrupt.

Therefore, it is clear in See that the interrupt itself causes the suspending operation and not any read command or request. The discussion of Figure 5 through 7 of See is consistent with these views. The read command itself in See does not cause suspension; the suspension occurs as a result of an interrupt. In See, the suspension operation occurs before the read operation. Therefore, to the extent recited in each independent claim on appeal, See cannot anticipate within 35 U.S.C. § 102 the subject matter of the independent claims on appeal. As such, the rejection of various dependent claims under 35 U.S.C. § 102 and 35 U.S.C. § 103 also cannot be sustained.

In summary, we have sustained the rejection of claims 29 and 30 under the written description portion of 35 U.S.C. § 112, first paragraph. On the other hand, we have reversed the rejection of the claims on appeal under 35 U.S.C. § 102 and 35 U.S.C. § 103. Since we have sustained at least one rejection of some of the claims on appeal, the decision of the examiner is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

JAMES D. THOMAS
Administrative Patent Judge

KENNETH W. HAIRSTON
Administrative Patent Judge

JOSEPH L. DIXON
Administrative Patent Judge

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) INTERFERENCES

JDT:psb

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